gridconnect

DSTni-EX User Guide

Section 1

Part Number 900-335
Revision A 3/04

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Contents

1: About This User Guide

This User Guide describes the technical features and programming interfaces of the Lantronix DSTni-EX chip (hereafter referred to as “DSTni”).

DSTni is an Application Specific Integrated Circuit (ASIC)-based single-chip solution (SCS) that integrates the leading-edge functionalities needed to develop low-cost, high-performance device server products. On a single chip, the DSTni integrates an x186 microprocessor, 16K-byte ROM, 256K-byte SRAM, programmable input/output (I/O), and serial, Ethernet, and Universal Serial Bus (USB) connectivity — key ingredients for device- server solutions. Although DSTni embeds multiple functions onto a single chip, it can be easily customized, based on the comprehensive feature set designed into the chip.

Providing a complete device server solution on a single chip enables system designers to build affordable, full-function solutions that provide the highest level of performance in both processing power and peripheral systems, while reducing the number of total system components. The advantages gained from this synergy include:

- Simplifying system design and increased reliability.
- Minimizing marketing and administration costs by eliminating the need to source products from multiple vendors.
- Eliminating the compatibility and reliability problems that occur when combining separate subsystems.
- Dramatically reducing implementation costs.
- Increasing performance and functionality, while maintaining quality and cost effectiveness.
- Streamlining development by reducing programming effort and debugging time.
- Enabling solution providers to bring their products to market faster.
- These advantages make DSTni the ideal solution for designs requiring x86 compatibility; increased performance; serial, programmable I/O, Ethernet, and USB communications; and a glueless bus interface.

Intended Audience

This User Guide is intended for use by hardware and software engineers, programmers, and designers who understand the basic operating principles of microprocessors and their systems and are considering designing systems that utilize DSTni.

Conventions

This User Guide uses the following conventions to alert you to information of special interest.

The symbols # and n are used throughout this Guide to denote active LOW signals.

Notes: *Notes are information requiring attention.*

Navigating Online

The electronic Portable Document Format (PDF) version of this User Guide contains *hyperlinks*. Clicking one of these hyper links moves you to that location in this User Guide. The PDF file was created with Bookmarks and active links for the Table of Contents, Tables, Figures and cross-references.

Organization

This User Guide contains information essential for system architects and design engineers. The information in this User Guide is organized into the following chapters and appendixes.

- *Section 1: Introduction*
  Describes the DSTni architecture, design benefits, theory of operations, ball assignments, packaging, and electrical specifications. This chapter includes a DSTni block diagram.
- *Section 2: Microprocessor*
  Describes the DSTni microprocessor and its control registers.
- *Section 2: SDRAM*
  Describes the DSTni SDRAM and the registers associated with it.
- *Section 3: Serial Ports*
  Describes the DSTni serial ports and the registers associated with them.
- *Section 3: Programmable Input/Output*
  Describes DSTni's Programmable Input/ Output (PIO) functions and the registers associated with them.
- *Section 3: Timers*
  Describes the DSTni timers.
- *Section 4: Ethernet Controllers*
  Describes the DSTni Ethernet controllers.
- *Section 4: Ethernet PHY*
  Describes the DSTni Ethernet physical layer core.
- *Section 5: SPI Controller*
  Describes the DSTni Serial Peripheral Interface (SPI) controller.
- *Section 5: I2C Controller*
  Describes the DSTni I^2C controller.
- *Section 5: USB Controller*
  Describes the DSTni USB controller.
- *Section 5: CAN Controllers*
  Describes the DSTni Controller Area Network (CAN) bus controllers.
- *Section 6: Interrupt Controller*
  Describes the DSTni interrupt controller.
- *Section 6: Miscellaneous Registers*
  Describes DSTni registers not covered in other chapters of this Guide.
- *Section 6: Debugging In-circuit Emulator (Delce)*
- *Section 6: Packaging and Electrical*
  Describes DSTni's packaging and electrical characteristics.
- *Section 6: Applications*
  Describes DSTni's packaging and electrical characteristics.
- *Section 6: Instruction Clocks*
  Describes the DSTni instruction clocks.
- *Section 6: DSTni Sample Code*
- *Section 6: Baud Rate Calculations*
  Provides baud rate calculation tables.

2: Introduction

Design Philosophy

DSTni is a cost-effective, high-performance solution that is the optimized for device server technology board products requiring x86 compatibility, increased performance, and serial, parallel, Ethernet, and/or Universal Serial Bus (USB) connectivity. DSTni integrates the functionality of today's cutting-edge technologies into a robust, cost-effective, embedded single-chip solution (SCS). This approach enables system designers to develop all-in-one, next-generation device server solutions around a single, flexible DSTni chip, with minimum silicon cost and design effort. In this way, DSTni makes it possible to implement a fully functional system — with ROM and RAM; serial, parallel, Ethernet, and USB interfaces; and programmable input/output (PIO) capability — without requiring additional system-interface logic.

DSTni's all-in-one SCS solution reduces development costs and time-to-market by integrating all of the functionality needed to build board-level device server solutions. Even manufacturers that lack the expertise or resources to enter the growing device server marketplace can use DSTni to gain a competitive edge in their market segment.

DSTni Architecture

At the heart of DSTni is an embedded enhanced 80186 microprocessor. As the most widely supported embedded computer architecture in the world, x86 fully leverages the installed base of software drivers, peripheral chips, networking, and communication protocol stacks, and real-time operating systems. It also has the widest performance range of any microprocessor, allowing for a broad range of system implementations and cost targets.

x86-based code inherently uses less memory than equivalent RISC-based code, so less physical memory is required in an end system for the same application. And because x86 is the same industry-standard architecture used on PCs, existing x86 assembly language can be ported to the DSTni with minimal modifications.

Note: *I/O registers and peripherals internal to DSTni are word registers unless otherwise defined. They should be only written as words. Peripherals outside DSTni can be written as either bytes or words.*

Feature List

- Embedded Phase Lock Loop (PLL) 1-115x
- Embedded enhanced 80186 CPU (1 to 115 MHz)
- Embedded enhanced 80186 peripherals
- Embedded Ethernet controllers
  - Enhanced 32-byte-deep transmit FIFOs
  - One MII interface port 0 with 10/100 Mbit PHY transceiver (includes 100Base-FX)
  - Second MII interface port 1
- Embedded boot code
  - 16K bytes of ROM (8K x 16)
- Embedded Synchronous Random Access Memory (SRAM)
  - 256K bytes of 0 wait state SRAM (128K x 16)
- Embedded Burst/Page Access Upper Chip Select (UCS)
- Four 186ES-compatible serial ports
  - Enhanced receive FIFOs (4 deep)
  - Additional handshake control
- Two CANBUS 2.0b controllers
- One Universal Serial Bus (USB) 1.1 Controller
- One 3-wire Serial Peripheral Interface (SPI) controller
- One 2-wire I^2C serial controller
- Single input clock (25 MHz)
- 16-bit random-number generator
- 16-bit TCP/IP checksum generator
- SDRAM memory interface (16, 64, and 128 Mbit)
- Temperature range: –40°C to 85°C ambient
- Package 12x12 mm 184 BGA

Feature Descriptions

Software-Controlled Clock

DSTni comes with a phase-lock loop that can be programmed from 1 to 115 MHz. This feature allows DSTni to be run at a variety of clock frequency combinations, up to 115 MHz, while keeping power consumption to an absolute minimum. The clock defaults to 24 MHz on power-up or reset. As a result, DSTni can be scaled to perform tasks at the speed ideally suited for those tasks, thereby minimizing power consumption and heat generation and conserving energy.

Small Footprint

DSTni has a footprint of 12 mm^2. DSTni's Ball Grid Array (BGA) package provides a significant reduction in board real estate. This allows DSTni to fit the most tightly populated products. DSTni also boasts a glueless logic architecture for a seamless hardware interface.

Four Asynchronous Serial Ports

DSTni provides four identical asynchronous serial ports. Each port operates independently and has the following features:

- Full-duplex operation
- Programmable baud-rate generator
- 7-, 8-, or 9-bit operation
- Even, odd, or no parity
- 1 or 2 stop bits:
  1 stop bit for 7-, 8-, or 9-bit operation
  2 stop bits for 7- or 8-bit operation
- Direct Memory Access (DMA) to and/or from serial ports
- Hardware flow control
- Transmit and detect break characters
- Programmable interrupt generation for break characters and data words

DMA and Serial Ports

Each DSTni serial port can use its own DMA channel, allowing for direct DMA to and from the serial port. DMA transfers to a serial port are destination synchronized; DMA transfers from a serial port are source synchronized, with a new request generated when data is present in the receive FIFO.

Note: *A total of 4 DMA channels are available. Typically, if four serial channels are used, one DMA channel is placed on each receive channel.*

Two Ethernet Controllers

DSTni supports two IEEE-compliant Ethernet controllers:

- One controller has the PHY transceiver connected to it. This controller works in 10/ 100 Mbit (10Base-T and 100Base-TX) mode and supports 100Base-FX mode (100 Mbit over two fiber-optic cables).
- The other controller has an external MII interface.

The internal PHY supports half- and full-duplex operation, with full-featured auto-negotiation functionality.

CANBUS 2.0b Controllers

DSTni provides two CANBUS 2.0b controllers that filter incoming messages by identifier or by data. Messages that do not pass the controller's filtering mechanism are not passed to the microprocessor, saving CPU bandwidth.

USB 1.1 Controller

DSTni supports a USB 1.1 controller, which is fully compliant as a device. The controller supports 8 bidirectional endpoints, along with DMA or First In First Out (FIFO) data stream interfaces. The USB controller also provides host-mode logic for emulating a PC host.

SPI Serial Controller

DSTni provides a 3-wire SPI serial controller that supports "master" and "slave" devices, as well as multiple-master and multiple-slave devices. The SPI interface detects collisions when multiple masters try to transfer data at the same time, and is completely software programmable.

I^2C Serial Controller

DSTni provides a 2-wire I^2C serial controller that provides an interface between the DSTni microprocessor and an I^2C bus. It can be used in applications involving I^2C bus devices, including those that use the I^2C bus as a board-level communications protocol.

The controller can be programmed to operate as either a master or slave device.

- In master mode, the controller performs the required arbitration for operation in multimaster systems.
- In slave mode, the controller can interrupt the microprocessor when it recognizes its own 7- or 10-bit address or the general call address.

Watchdog Timer

DSTni provides a watchdog timer that can be configured to generate either an NMI interrupt or a system reset upon timeout. After reset, the watchdog timer defaults to the setting specified by bit [12] of the DSTni Configuration register (see page **Error! Bookmark not defined.**). It can be modified or disabled only one time.

If the timer is not disabled, the application program must periodically reset the timer by writing a specific key sequence to the watchdog timer control register. If the timer is not reset before it counts down, either an NMI or a system reset is issued, depending on the configuration of the timer.

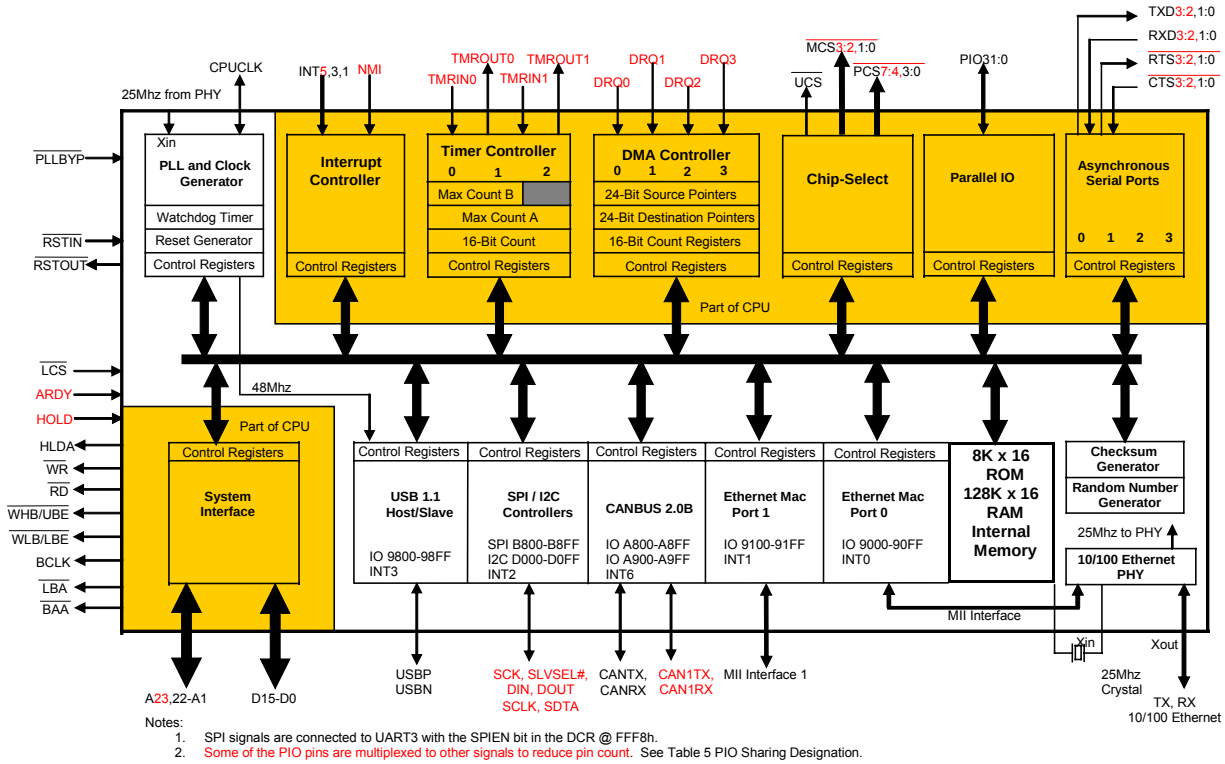
Standards Compliance

DSTni supports multiple worldwide standards including:

- IEEE 802.3, 802.3u, and 802.3af Ethernet standards
- CANBUS 2.0b
- USB 1.1

Block Diagram

Figure 2-1. DSTni Block Diagram

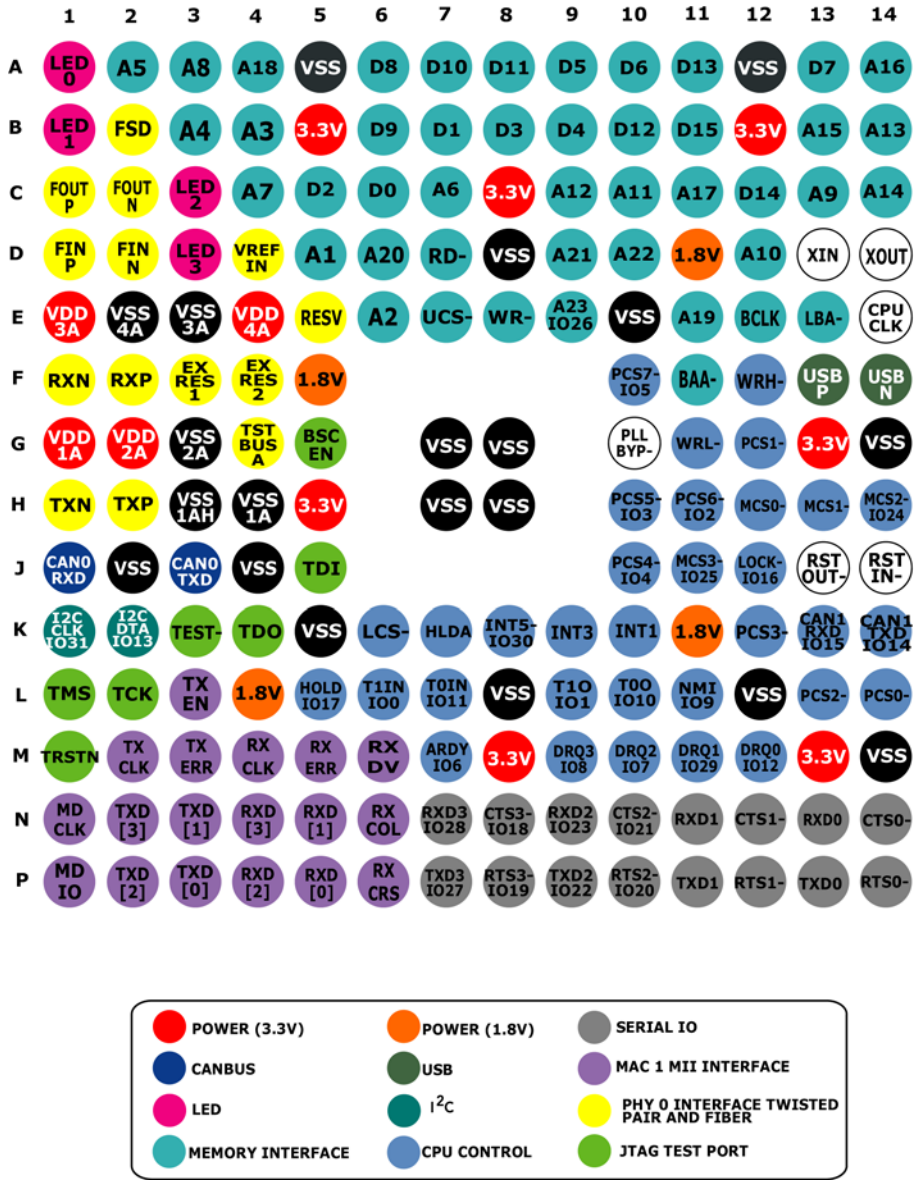


Notes:
1. SPI signals are connected to UART3 with the SPIEN bit in the DCR @ FFF8h.
2. Some of the PIO pins are multiplexed to other signals to reduce pin count. See Table 5 PIO Sharing Designation.

Ball Assignments

DSTni Ball Diagram

Figure 2-2. DSTni Ball Grid Array Looking through Top of Package



DSTni Ball Descriptions

Table 2-1. DSTni Ball Descriptions by Pin Name

Ball Pin Name	Ball Pin	Type	Description
Host Interface (All Pins are 5 Volt Tolerant)			
CPUCLK	E14	I/O	**CPU Clock Output** (24ma) This pin is driven from the output of the internal PLL. This output pin can be three-stated by setting the CD bit in the SYSCON register. When the PLL is bypassed, this pin is tri-stated and is the CPUCLK input source.
PLLBYP#	G10	IN	**PLL Bypass Input** (Active LOW with Pull-up) This input, when pulled LOW, bypasses the internal PLL and uses the CPUCLK pin as the source for the CPU.
WR#	E8	OUT	**Write Output** (16ma Active LOW with Pull-up) This pin indicates that the current bus cycle is a memory or I/O write cycle.
RD#	D7	I/O	**Read Output** (16ma Active LOW with Pull-up) This pin indicates that the current bus cycle is a memory or I/O read cycle. If HLDA is active, this pin is used as an input to read data from the internal 256K bytes of SRAM.
WRH#	F12	I/O	**Write High Output** (16ma Active Low with Pull-up) IF CSBE is set to '1' in the DCR, this pin indicates that the current bus cycle is a memory or I/O write cycle and that the upper byte is being driven with valid data. IF CSBE is set to '0' in the DCR, this pin indicates the upper byte chip select is valid. If HLDA is active, this pin is used as an input to enable writing data to the upper byte of the internal 256K bytes of SRAM.
WRL#	G11	I/O	**Write Low Output** (16ma Active LOW with Pull-up) IF CSBE is set to '1' in the DCR, this pin indicates that the current bus cycle is a memory or I/O write cycle and that the lower byte is being driven with valid data. If CSBE is set to '0' in the DCR, this pin indicates the lower byte chip select is valid. If HLDA is active, this pin is used as an input to enable writing data to the lower byte of the internal 256K bytes of SRAM.
UCS#	E7	OUT	**Upper Memory Chip Select Output** (4ma Active LOW) This pin indicates to the system that a memory access is in progress to the upper memory block. The base address and size of the upper memory block are programmable up to 1 Mbyte (20-bit address mode) or up to 16 Mbyte (24-bit address mode). Upper memory chip select is always configured for 16bit bus size. After reset, UCS# is active for the 64 Kbyte memory range from F0000h to FFFFFh (20-bit address mode) or from FF0000h to FFFFFFh (24-bit address mode).
HLDA	K7	OUT	**Hold Acknowledge** (4ma Active HIGH) This pin goes HIGH to indicate the bus has been released for use by an external bus master. The internal 256K bytes of internal memory is the only peripheral that can be accessed by an external bus master. The bus is requested using the HOLD pin (multiplexed on IO17).
LCS#	K6	IN	**Lower Chip Select** (Schmitt Trigger Input Active LOW with Pull-up) This pin is used by an external bus master to enable reading and writing the internal 256K bytes of SRAM.
LBA#	E13	OUT	**Load Burst Address Output** (12ma Active LOW) This pin, when LOW, causes the burst flash memory device to load a new memory address from which to access memory cycles. This means a burst miss has occurred.
BAA#	F11	OUT	**Burst Address Advance Output** (12ma Active LOW) This pin, when LOW, causes the burst flash memory device to increment the internal memory address from which to access memory cycles. This means a burst hit has occurred.

Ball Pin Name	Ball Pin	Type	Description
BCLK	E12	OUT	**Burst Clock Output** (12ma Active HIGH) This pin, when clocking from LOW to HIGH, causes the burst flash memory device to process any commands determined by the LBA# or BAA# pins. This pin only transitions when burst flash is enabled and one of the flash control signals has changed.
MCS[1]# MCS[0]#	H13 H12	OUT OUT	**Middle Memory Chip Select Output** (8ma Active LOW) These pins indicate to the system that a memory access is in progress to the midrange memory block. The base address and size of the mid-range memory block are programmable. The Middle memory chip selects are always configured for 16bit bus size. MCS[0]# can be programmed as the chip select for the entire middle chip select address range. MCS[0] is also used as CS_n for connecting a SDRAM externally.
PCS[3]# PCS[2]# PCS[1]# PCS[0]#	K12 L13 G12 L14	OUT OUT OUT OUT	**Peripheral Chip Select Output** (8ma Active LOW) These pins indicate to the system that a bus cycle is in progress to the corresponding region of the peripheral space. The base address of the peripheral block is programmable.
RSTIN#	J14	IN	**Reset Input** (Schmitt Trigger Input, Active LOW with Pull-up) This pin causes the CPU to perform a reset. When this pin is asserted, the CPU immediately terminates any current bus cycles, resets internal logic and prepares for executing code at the reset address. FFFF0h in 20bit mode and FFFFE0h in 24bit mode. RSTIN# is synchronized internally and extended internally to allow ~200 ms for the DCR and RCR to settle to the values driven by there individual resistors. This input is provided with a Schmitt trigger to power-on via an RC network.
RSTOUT#	J13	OUT	**Reset Output** (4ma Active LOW) This pin indicates whether the CPU is being reset. It indicates that the internal logic is being reset and is to be used to reset any external peripherals.
DB[15] DB[14] DB[13] DB[12] DB[11] DB[10] DB[9] DB[8] DB[7] DB[6] DB[5] DB[4] DB[3] DB[2] DB[1] DB[0]	B11 C12 A11 B10 A8 A7 B6 A6 A13 A10 A9 B9 B8 C5 B7 C6	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-downs) These pins supply the data to the memory or I/O of the system. The state of these pins are also latched into the Reset Configuration Register (RCR) prior to RSTOUT being de-asserted. External pull-up resistors can be placed on this bus to set the corresponding bit in the RCR.

<table>
<tr><th>Ball Pin Name</th><th>Ball Pin</th><th>Type</th><th>Description</th></tr>
<tr><td>A[22]
A[21]
A[20]
A[19]
A[18]
A[17]
A[16]
A[15]
A[14]
A[13]
A[12]
A[11]
A[10]
A[9]
A[8]
A[7]
A[6]
A[5]
A[4]
A[3]
A[2]
A[1]</td><td>D10
D9
D6
E11
A4
C11
A14
B13
C14
B14
C9
C10
D12
C13
A3
C4
C7
A2
B3
B4
E6
D5</td><td>I/O 1
I/O 1
I/O 1
I/O 0
I/O 0
I/O 0
I/O 0
I/O 1
I/O 1
I/O 1
I/O 1
I/O 0
I/O 0
I/O 0
I/O 0
I/O 0
I/O 0
I/O 0
I/O 0
I/O 0
I/O 0
I/O 0</td><td>Address Bus (8ma with Pull-ups and Pull-downs)
These pins supply the address to memory or I/O of the system. If HLDA is active, A17-1 are used to access the internal 256K bytes of internal SRAM. The other address pins are ignored.
Just prior to RSTOUT being de-asserted, these pins program the DCR register.
<table><tr><th>A22</th><th>BOOTROM</th><th>Default</th></tr><tr><td>0</td><td>Disabled</td><td></td></tr><tr><td>1</td><td>Enabled</td><td>*</td></tr></table><table><tr><th>A21</th><th>Address Mode</th><th>Default</th></tr><tr><td>0</td><td>20 Bit</td><td></td></tr><tr><td>1</td><td>24 Bit</td><td>*</td></tr></table><table><tr><th>A20</th><th>Watchdog</th><th>Default</th></tr><tr><td>0</td><td>Disabled</td><td></td></tr><tr><td>1</td><td>Enabled</td><td>*</td></tr></table><table><tr><th>A18</th><th>SPI</th><th>Default</th></tr><tr><td>0</td><td>Disabled</td><td>*</td></tr><tr><td>1</td><td>Enabled</td><td></td></tr></table>A19, [17:8] are used in various ways by internal boot routines.
A7-1 are used for ASIC production testing only. Leave at ‘0’.
In 20-bit address mode, A20-23 are not used and return '0'.
In 20-bit address mode, A20-23 always return '0' during code execution.</td></tr>
<tr><td>INT3
INT1</td><td>K9
K10</td><td>IN
IN</td><td>Interrupt In (Schmitt Trigger Input, Active HIGH with Pull-down)
These pins are external interrupt input requests. INT3 is OR’ed with the USB controller at interrupt type 15. INT1 is OR’ed with the MAC 1 controller at interrupt type 13.</td></tr>
<tr><td colspan="4">UART0 Interface</td></tr>
<tr><td>TXD0</td><td>P13</td><td>OUT</td><td>Transmit Data 0 Out (2ma)
This pin provides serial transmit data to the system from serial port 0.</td></tr>
<tr><td>RXD0</td><td>N13</td><td>IN</td><td>Receive Data 0 In (Schmitt Trigger Input, Active HIGH with Pull-up)
This pin provides serial receive data from the system to serial port 0.</td></tr>
<tr><td>RTS0#</td><td>P14</td><td>OUT</td><td>Ready to Send 0 Out (2ma)
This pin provides the Ready to Send output for serial port 0. This pin provides the handshaking output for serial port 0.</td></tr>
<tr><td>CTS0#</td><td>N14</td><td>IN</td><td>Clear to Send 0 In (Schmitt Trigger Input, Active High with Pull up)
This pin provides the Clear to Send input for serial port 0. This pin provides the handshaking input for serial port 0.</td></tr>
<tr><td colspan="4">UART1 Interface</td></tr>
<tr><td>TXD1</td><td>P11</td><td>OUT</td><td>Transmit Data 1 Out (2ma)
This pin provides serial transmit data to the system from serial port 1.</td></tr>
<tr><td>RXD1</td><td>N11</td><td>IN</td><td>Receive Data 1 In (Schmitt Trigger Input, Active HIGH with Pull-up)
This pin provides serial receive data from the system to serial port 1.</td></tr>
<tr><td>RTS1#</td><td>P12</td><td>OUT</td><td>Ready to send 1 Out (2ma)
This pin provides the Ready to Send output for serial port 1. This pin provides the handshaking output for serial port 1.</td></tr>
<tr><td>CTS1#</td><td>N12</td><td>IN</td><td>Clear to Send 1 In (Schmitt Trigger Input, Active HIGH with Pull-up)
This pin provides the Clear to Send input for serial port 1. This pin provides the handshaking input for serial port 1.</td></tr>
<tr><td colspan="4">Parallel Interface</td></tr>
<tr><td>PIO31
I2CCLK</td><td>K1</td><td>I/O
I/O</td><td>Parallel I/O Bit [31] Pin (4ma Schmitt Input with Pull-up)
This pin corresponds to bit [31] of the PIO register.
This pin can also be used with the I^2C block as the CLK if PIO bit [31] is programmed for normal operation.</td></tr>
</table>

Ball Pin Name	Ball Pin	Type	Description
PIO30 INT5#	K8	I/O IN	**Parallel I/O Bit [30] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [30] of the PIO register. This pin can also be used as INT5 when PIO30 is programmed for normal operation. **Note: This interrupt is shared with UART 3.**
PIO29 DRQ1	M11	I/O IN	**Parallel I/O Bit [29] and DRQ1 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [29] of the PIO register. This pin can also be used as DMA request 1 with the DMA if PIO bit [29] is programmed for normal operation.
PIO28 RXD3 MOSI	N7	I/O IN OUT	**Parallel I/O Bit [28] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [28] of the PIO register. This pin can also be used with: ● UART 3 as receive data (RXD3) if PIO bit [28] is programmed for normal operation. ● The SPI controller if the SPIEN bit is set in the DCR register. This pin connects to the serial data in (SDI) of an external SPI device.
PIO27 TXD3 MISO	P7	I/O OUT IN	**Parallel I/O Bit [27] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [27] of the PIO register. This pin can also be used with: ● UART 3 as transmit data (TXD3) if PIO bit [27] is programmed for normal operation. ● The SPI controller if the SPIEN bit is set in the DCR register. This pin connects to the serial data out (SDO) of an external SPI device.
PIO26 A23	E9	I/O OUT	**Parallel I/O Bit [26] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [26] of the PIO register. This pin can also be used as address line 23 (A23) if PIO bit [26] is programmed for normal operation.
PIO25 MCS3#	J11	I/O OUT	**Parallel I/O Bit [25] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [25] of the PIO register. This pin can also be used as middle chip select 3 (MCS3#) if PIO bit [25] is programmed for normal operation.
PIO24 MCS2#	H14	I/O OUT	**Parallel I/O Bit [24] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [24] of the PIO register. This pin can also be used as middle chip select 2 (MCS2#) if PIO bit [24] is programmed for normal operation.
PIO23 RXD2	N9	I/O IN	**Parallel I/O Bit [23] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [23] of the PIO register. This pin can also be used with UART 2 as receive data (RXD2) if PIO bit [23] is programmed for normal operation.
PIO22 TXD2	P9	I/O OUT	**Parallel I/O Bit [22] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [22] of the PIO register. This pin can also be used with UART 2 as transmit data (TXD2) if PIO bit [22] is programmed for normal operation.
PIO21 CTS2#	N10	I/O IN	**Parallel I/O Bit [21] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [21] of the PIO register. This pin can also be used with UART 2 as Clear to Send (CTS2#) if PIO bit [21] is programmed for normal operation.
PIO20 RTS2#	P10	I/O OUT	**Parallel I/O Bit [20] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [20] of the PIO register. This pin can also be used with UART 2 as ready to send (RTS2#) if PIO bit [20] is programmed for normal operation.
PIO19 RTS3# SCK	P8	I/O OUT I/O	**Parallel I/O Bit [19] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [19] of the PIO register. This pin can also be used with: ● UART 3 as ready to send (RTS3#) if PIO bit [19] is programmed for normal operation. ● The SPI controller if the SPIEN bit is set in the DCR register. This pin connects to the serial clock (SCK) of the SPI controller.

Ball Pin Name	Ball Pin	Type	Description
PIO18 CTS3# SLVSEL	N8	I/O IN IN	**Parallel I/O Bit [18] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [18] of the PIO register. This pin can also be used with: ● UART 3 as clear to send (CTS3#) if PIO bit [18] is programmed for normal operation. ● The SPI controller if the SPIEN bit is set in the DCR register. This pin connects to the slave select output (SLVSEL) of the SPI controller.
PIO17 HOLD	L5	I/O IN	**Parallel I/O Bit [17] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [17] of the PIO register. This pin can also be used as the HOLD input if PIO bit [17] is programmed for normal operation. When driven HIGH by an external bus master, the CPU responds with HLDA and releases the bus for external use. Only the internal 256K bytes of memory are accessible externally.
PIO16 LOCK# SRDYOUT	J12	I/O OUT OUT	**Parallel I/O Bit [16] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [16] of the PIO register. This pin can also be used as the CPU bus lock# output. If the SRDYOUT bit in the PLL/CLK register is set to '1', this pin outputs the internal SRDY signal for wait state debug use.
PIO15 CAN1RXD	K13	I/O IN	**Parallel I/O Bit [15] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [15] of the PIO register. This pin can also be used as CAN controller 1 receive if PIO bit [15] is programmed for normal operation.
PIO14 CAN1TXD	K14	I/O OUT	**Parallel I/O Bit [14] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [14] of the PIO register. This pin can also be used as CAN controller 1 transmit if PIO bit [14] is programmed for normal operation.
PIO13 I2CDTA	K2	I/O	**Parallel I/O Bit [13] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [13] of the PIO register. This pin can also be used with the I^2C block as the I2CDTA if PIO bit [13] is programmed for normal operation.
PIO12 DRQ0	M12	I/O IN	**Parallel I/O Bit 12 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [12] of the PIO register. This pin can also be used with DMA channel 0 as DRQ0 if PIO bit [12] is programmed for normal operation.
PIO0 TMR1IN	L6	I/O IN	**Parallel I/O Bit [0] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [0] of the PIO register. This pin can also be used with Timer Channel 1 as TMR1IN if PIO bit [0] is programmed for normal operation.
PIO11 TMR0IN	L7	I/O IN	**Parallel I/O Bit 11 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [11] of the PIO register. This pin can also be used with Timer Channel 0 as TMR0IN if PIO bit [11] is programmed for normal operation.
PIO10 TMR0OUT	L10	I/O OUT	**Parallel I/O Bit [10] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [10] of the PIO register. This pin can also be used with Timer Channel 0 as TMR0OUT if PIO bit [10] is programmed for normal operation.
PIO9 NMI	L11	I/O IN	**Parallel I/O Bit [9] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [9] of the PIO register. This pin can also be used with NMI input if PIO bit [9] is programmed for normal operation.
PIO8 DRQ3	M9	I/O IN	**Parallel I/O Bit [8] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [8] of the PIO register. This pin can also be used with DMA channel 3 as DRQ3 if PIO bit [8] is programmed for normal operation.
PIO7 DRQ2	M10	I/O IN	**Parallel I/O Bit [7] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [7] of the PIO register. This pin can also be used with DMA channel 2 as DRQ2 if PIO bit [7] is programmed for normal operation.

Ball Pin Name	Ball Pin	Type	Description
PIO6 ARDY	M7	I/O IN	**Parallel I/O Bit 6 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [6] of the PIO register. This pin can also be used with an external ready source ARDY if PIO bit [6] is programmed for normal operation. ARDY is double synchronized internally using the falling edge of CPUCLK. It can be used to extend external accesses if enabled by the appropriate registers (External Ready).
PIO5 PCS7#	F10	I/O OUT	**Parallel I/O Bit [5] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [5] of the PIO register. This pin can also be used as peripheral chip select 7 (PCS7#) if PIO bit [5] is programmed for normal operation.
PIO4 PCS4#	J10	I/O OUT	**Parallel I/O bit 4 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [4] of the PIO register. This pin can also be used as peripheral chip select 4 (PCS4#) if PIO bit [4] is programmed for normal operation.
PIO3 PCS5#	H10	I/O OUT	**Parallel I/O Bit [3] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [3] of the PIO register. This pin can also be used as peripheral chip select 5 (PCS5#) if PIO bit [3] is programmed for normal operation.
PIO2 PCS6#	H11	I/O OUT	**Parallel I/O Bit [2] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [2] of the PIO register. This pin can also be used as peripheral chip select 6 (PCS6#) if PIO bit [2] is programmed for normal operation.
PIO1 TMR1OUT	L9	I/O OUT	**Parallel I/O bit [1] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [1] of the PIO register. This pin can also be used with Timer Channel 1 as TMR1OUT if PIO bit [1] is programmed for normal operation.
CAN Bus 0 Interface (External Transceiver)			
CANTXD	J3	OUT	**CAN Transmit** (2ma) This pin connects to an external CAN transceiver transmit pin.
CANRXD	J1	IN	**CAN Receiver** (Schmitt Input with Pull-up) This pin connects to an external CAN transceiver receive pin.
USB Interface			
USBP	F13	I/O	**USB 1.1 Plus** USB Transceiver Positive Signal
USBN	F14	I/O	**USB 1.1 Negative** USB Transceiver Negative Signal
Ethernet 0 Interface (Internal PHY)			
XIN XOUT	D13 D14	IN OUT	**Ethernet Clock** (25 MHz Crystal) These pins provide the connections for a fundamental mode parallel-resonant crystal.
LED0	A1	OUT	**LED0 Driver** (8ma)
LED1	B1	OUT	**LED1 Driver** (8ma)
LED2	C3	OUT	**LED2 Driver** (8ma)
LED3	D3	OUT	**LED3 Driver** (8ma)
TXP	H2	OUT	**Ethernet Transmit Plus**
TXN	H1	OUT	**Ethernet Transmit Negative**
RXP	F2	IN	**Ethernet Receive Plus**
RXN	F1	IN	**Ethernet Receive Negative**
EXRES1	F3	I/O	**Ethernet Current Source 1** (12.4K 1% resistor Pin1)
EXRES2	F4	I/O	**Ethernet Current Source 2** (12.4K 1% resistor Pin 2)
TSTBUSA	G4	I/O	**Test BUS A** (for factory testing of PHY only; leave unconnected)

Ball Pin Name	Ball Pin	Type	Description
Ethernet 0 Fiber Interface (Internal PHY)			
FSD	B2	IN	**Fiber Signal Detect** (Schmitt Trigger Input with Pull-down)
FOUTP	C1	OUT	**Fiber Transmit Data Plus** (PECL voltage levels)
FOUTN	C2	OUT	**Fiber Transmit Data Negative** (PECL voltage levels)
FINP	D1	IN	**Fiber Receive Data Plus** (PECL voltage levels)
FINN	D2	IN	**Fiber Receive Data Negative** (PECL voltage levels)
RESV	E5	IN	**Reference Current Resistor Input** (1.24K 1% resistor to VSS)
VREF	D4	IN	**Voltage Reference Input** (1.235V reference voltage)
PHY Power (Internal PHY)			
VDD1A	G1	PWR	**Power I/O**: +3.3 volt power supply (requires a separate via to power plane)
VDD2A	G2	PWR	**Power I/O**: +3.3 volt power supply (requires a separate via to power plane)
VDD3A	E1	PWR	**Power I/O**: +3.3 volt power supply (requires a separate via to power plane)
VDD4A	E4	PWR	**Power I/O**: +3.3 volt power supply (requires a separate via to power plane)
VSS1A(H)	H3	PWR	**Power GND**: +3.3 volt power supply (100ma sink capability) (requires a separate via to power plane)
VSS1A	H4	PWR	**Power GND**: +3.3 volt power supply (requires a separate via to power plane)
VSS2A	G3	PWR	**Power GND**: +3.3 volt power supply (requires a separate via to power plane)
VSS3A	E3	PWR	**Power GND**: +3.3 volt power supply (requires a separate via to power plane)
VSS4A	E2	PWR	**Power GND**: +3.3 volt power supply (requires a separate via to power plane)
MII Ethernet 1 Interface (External PHY) All bi-directional during factory testing			
MDIO	P1	I/O	**Ethernet MII 1 Management Data** (4ma with Input and Pull-down)
MDC	N1	OUT	**Ethernet MII 1 Clock Out** (4ma with Input and Pull-down)
TXCLK	M2	IN	**Ethernet Transmit Clock** (4ma with Input and Pull-down)
TXEN	L3	OUT	**Ethernet Transmit Enable** (4ma with Input and Pull-down)
TXER	M3	OUT	**Ethernet Transmit Error** (4ma with Input and Pull-down)
TXD[3]	N2	OUT	**Ethernet Transmit Data Bus Bit [3]** (4ma with input and Pull-down)
TXD[2]	P2	OUT	**Ethernet Transmit Data Bus Bit [2]** (4ma with input and Pull-down)
TXD[1]	N3	OUT	**Ethernet Transmit Data Bus Bit [1]** (4ma with Input and Pull-down)
TXD[0]	P3	OUT	**Ethernet Transmit Data Bus Bit [0]** (4ma with Input and Pull-down)
RXCLK	M4	IN	**Ethernet Receive Clock** (4ma with Input and Pull-down)
RXDV	M6	IN	**Ethernet Receive Data Valid** (4ma with input and Pull-down)
RXER	M5	IN	**Ethernet Receive Error** (4ma with Input and Pull-down)
RXD[3]	N4	IN	**Ethernet Receive Data Bus Bit [3]** (4ma with Input and Pull-down)
RXD[2]	P4	IN	**Ethernet Receive Data Bus Bit [2]** (4ma with input and Pull-down)
RXD[1]	N5	IN	**Ethernet Receive Data Bus Bit [1]** (4ma with input and Pull-down)
RXD[0]	P5	IN	**Ethernet Receive Data Bus Bit [0]** (4ma with input and Pull-down)
RXCRS	P6	IN	**Ethernet Receive Carrier Sense** (4ma with Input and Pull-down)
RXCOL	N6	IN	**Ethernet Receive Collision** (4ma with Input and Pull-down)

Ball Pin Name	Ball Pin	Type	Description
Test (Internal Factory Test Modes)			
TCK	L2	IN	**Test Clock** (Schmitt Trigger Input and Pull-up)
TDI	J5	IN	**Test Data Input** (Schmitt Trigger Input and Pull-up)
TDO	K4	OUT	**Test Data Output** (4ma)
TMS	L1	IN	**Test Mode Select** (Schmitt Trigger Input and Pull-up)
TRST#	M1	IN	**Test Reset** (Schmitt Trigger Input and Pull-up)
BSCEN	G5	IN	**TEST TAP Select** (Schmitt Trigger Input and Pull-up) This pin can be left high to enable the internal boundary scan tap control. When pulled low the internal JTAG debugger is enabled.
TEST#	K3	IN	**TEST pin** (Schmitt Trigger Input and Pull-up) When this pin is pulled LOW, internal test modes may be input using address line 1 to 7. When HIGH, test is disabled.
Power			
VDD1.8	D11	PWR	Power Core: +1.8 volt power supply
VDD1.8	F5	PWR	Power Core: +1.8 volt power supply
VDD1.8	L4	PWR	Power Core: +1.8 volt power supply
VDD1.8	K11	PWR	Power Core: +1.8 volt power supply
VSS	A5	PWR	Power VSS
VSS	A12	PWR	Power VSS
VSS	D8	PWR	Power VSS
VSS	E10	PWR	Power VSS
VSS	G14	PWR	Power VSS
VSS	J2	PWR	Power VSS
VSS	J4	PWR	Power VSS
VSS	K5	PWR	Power VSS
VSS	L8	PWR	Power VSS
VSS	L12	PWR	Power VSS
VSS	M14	PWR	Power VSS
VSS	G7	PWR	Power VSS (Thermal Ball)
VSS	G8	PWR	Power VSS (Thermal Ball)
VSS	H7	PWR	Power VSS (Thermal Ball)
VSS	H8	PWR	Power VSS (Thermal Ball)
VDD3.3	B5	PWR	Power I/O: +3.3 volt power supply
VDD3.3	B12	PWR	Power I/O: +3.3 volt power supply
VDD3.3	C8	PWR	Power I/O: +3.3 volt power supply
VDD3.3	G13	PWR	Power I/O: +3.3 volt power supply
VDD3.3	H5	PWR	Power I/O: +3.3 volt power supply
VDD3.3	M8	PWR	Power I/O: +3.3 volt power supply
VDD3.3	M13	PWR	Power I/O: +3.3 volt power supply

Pin Descriptions by Ball Designation

Table 2-2. DSTni Pin Descriptions by Ball Designation

Ball	Pin Name	Type	Description
A1	LED0	OUT	**LED0 Driver** (8ma)
A2	A[5]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
A3	A[8]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
A4	A[18]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
A5	VSS	PWR	**Power VSS**
A6	DB[8]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
A7	DB[10]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
A8	DB[11]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
A9	DB[5]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
A10	DB[6]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
All	DB[13]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
A12	VSS	PWR	**Power VSS**
A13	DB[7]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7. See Table 2-1 on page 2-7.
A14	A[16]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
B1	LED1	OUT	**LED1 Driver** (8ma)
B2	FSD	IN	**Fiber Signal Detect**
B3	A[4]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
B4	A[3]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
B5	VDD3.3	PWR	**Power I/O**: +3.3 volt power supply
B6	DB[9]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
B7	DB[1]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
B8	DB[3]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
B9	DB[4]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
B10	DB[12]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
Bll	DB[15]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
B12	VDD3.3	PWR	**Power I/O**: +3.3 volt power supply
B13	A[15]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
B14	A[13]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
C1	FOUTP	OUT	**Fiber Transmit Data Plus**
C2	FOUTN	OUT	**Fiber Transmit Data Negative**
C3	LED2	OUT	**LED2 Driver** (8ma)

Ball	Pin Name	Type	Description
C4	A[7]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
C5	DB[2]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
C6	DB[0]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
C7	A[6]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
C8	VDD3.3	PWR	**Power I/O**: +3.3 volt power supply
C9	A[12]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
C10	A[11]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
C11	A[17]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
C12	DB[14]	I/O	**CPU Data Bus** (8ma Active HIGH with Pull-down) See Table 2-1 on page 2-7.
C13	A[9]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
D1	FINP	IN	**Fiber Receive Data Plus**
D2	FINN	IN	**Fiber Receive Data Negative**
D3	LED3	OUT	**LED3 driver** (8ma)
D4	VREF	IN	**Voltage Reference Input** (1.235V reference voltage)
D5	A[1]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
D6	A[20]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
D7	RD#	I/O	**Read Output** (16ma Active LOW with Pull-up) This pin indicates that the current bus cycle is a memory or I/O read cycle. If HLDA is active, this pin is used as an input to read data from the internal 256K bytes of SRAM.
D8	VSS	PWR	**Power VSS**
D9	A[21]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
D10	A[22]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
D11	VDD1.8	PWR	**Power Core**: +1.8 volt power supply
D12	A[10]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
D13	XIN	IN	**Ethernet Clock** (25 MHz Crystal) These pins provide the connections for a fundamental mode parallel-resonant crystal.
D14	XOUT	OUT	

Ball	Pin Name	Type	Description
E1	VDD3A	PWR	**Power I/O**: +3.3 volt power supply (requires a separate via to power plane)
E2	VSS4A	PWR	**Power GND**: +3.3 volt power supply (requires a separate via to power plane)
E3	VSS3A	PWR	**Power GND**: +3.3 volt power supply (requires a separate via to power plane)
E4	VDD4A	PWR	**Power I/O**: +3.3 volt power supply (requires a separate via to power plane)
E5	RESV	IN	**Reference Current Resistor Input** (1.24K 1% resistor to VSS)
E6	A[2]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
E7	UCS#	OUT	**Upper Memory Chip Select Output** (4ma Active LOW) This pin indicates to the system that a memory access is in progress to the upper memory block. The base address and size of the upper memory block are programmable up to 1 Mbyte (20-bit address mode) or up to 16 Mbyte (24-bit address mode). Upper memory chip select is always configured for 16bit bus size. After reset, UCS# is active for the 64 Kbyte memory range from F0000h to FFFFFh (20-bit address mode) or from FF0000h to FFFFFFh (24-bit address mode).
E8	WR#	OUT	**Write Output** (16ma Active LOW with Pull-up) This pin indicates that the current bus cycle is a memory or I/O write cycle.
E9	PIO26 A23	I/O OUT	**Parallel I/O Bit [26] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [26] of the PIO register. This pin can also be used as address line 23 (A23) if PIO bit [26] is programmed for normal operation.
E10	VSS	PWR	**Power VSS**
E11	A[19]	I/O 0	**Address Bus** (8ma with Pull-ups and Pull-down) See Table 2-1 on page 2-7.
E12	BCLK	OUT	**Burst Clock Output** (12ma Active HIGH) This pin, when clocking from LOW to HIGH, causes the burst flash memory device to process any commands determined by the LBA# or BAA# pins. This pin only transitions when burst flash is enabled and one of the flash control signals has changed.
E13	LBA#	OUT	**Load Burst Address Output** (12ma Active LOW) This pin, when LOW, causes the burst flash memory device to load a new memory address from which to access memory cycles. This means a burst miss has occurred.
E14	CPUCLK	I/O	**CPU Clock Output** (24ma) This pin is driven from the output of the internal PLL. This output pin can be three-stated by setting the CD bit in the SYSCON register. When the PLL is bypassed, this pin is tri-stated and is the CPUCLK input source.
F1	RXN	IN	**Ethernet Receive Negative**
F2	RXP	IN	**Ethernet Receive Plus**
F3	EXRES1	I/O	**Ethernet Current Source 1** (12.4K 1% resistor Pin1)
F4	EXRES2	I/O	**Ethernet Current Source 2** (12.4K 1% resistor Pin 2)
F5	VDD1.8	PWR	**Power Core**: +1.8 volt power supply
F10	PIO5 PCS7#	I/O OUT	**Parallel I/O Bit [5] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [5] of the PIO register. This pin can also be used as peripheral chip select 7 (PCS7#) if PIO bit [5] is programmed for normal operation.
F11	BAA#	OUT	**Burst Address Advance Output** (12ma Active LOW) This pin, when LOW, causes the burst flash memory device to increment the internal memory address from which to access memory cycles. This means a burst hit has occurred.

Ball	Pin Name	Type	Description
F12	WRH#	I/O	**Write High Output** (16ma Active Low with Pull-up) IF CSBE is set to '1' in the DCR, this pin indicates that the current bus cycle is a memory or I/O write cycle and that the upper byte is being driven with valid data. IF CSBE is set to '0' in the DCR, this pin indicates the upper byte chip select is valid. If HLDA is active, this pin is used as an input to enable writing data to the upper byte of the internal 256K bytes of SRAM.
F13	USBP	I/O	**USB 1.1 Plus** USB Transceiver Positive Signal
F14	USBN	I/O	**USB 1.1 Negative** USB Transceiver Negative Signal
G1	VDD1A	PWR	**Power I/O**: +3.3 volt power supply (requires a separate via to power plane)
G2	VDD2A	PWR	**Power I/O**: +3.3 volt power supply (requires a separate via to power plane)
G3	VSS2A	PWR	**Power GND**: +3.3 volt power supply (requires a separate via to power plane)
G4	TSTBUSA	I/O	**Test BUS A** (testing only)
G5	BSCEN	IN	**TEST TAP Select** (Schmitt Trigger Input and Pull-up) This pin can be pulled LOW to enable the internal boundary scan tap control. When HIGH the internal JTAG debugger is enabled.
G7	VSS	PWR	**Power VSS** (Thermal Ball)
G8	VSS	PWR	**Power VSS** (Thermal Ball)
G10	PLLBYP#	IN	**PLL Bypass Input** (Active LOW with Pull-up) This input when pulled LOW bypasses the internal PLL and uses the CPUCLK pin as the source for the CPU.
G11	WRL#	I/O	**Write Low Output** (16ma Active LOW with Pull-up) IF CSBE is set to '1' in the DCR, this pin indicates that the current bus cycle is a memory or I/O write cycle and that the lower byte is being driven with valid data. If CSBE is set to '0' in the DCR, this pin indicates the lower byte chip select is valid. If HLDA is active, this pin is used as an input to enable writing data to the lower byte of the internal 256K bytes of SRAM.
G12	PCS[1]#	OUT	**Peripheral Chip Select Output** (8ma Active LOW) These pins indicate to the system that a bus cycle is in progress to the corresponding region of the peripheral space. The base address of the peripheral block is programmable.
G13	VDD3.3	PWR	**Power I/O: +3.3 Volt Power Supply**
G14	VSS	PWR	**Power VSS**
H1	TXN	OUT	**Ethernet Transmit Negative**
H2	TXP	OUT	**Ethernet Transmit Plus**
H3	VSS1A(H)	PWR	**Power GND**: +3.3 volt power supply (100ma sink capability) (requires a separate via to power plane)
H4	VSS1A	PWR	**Power GND**: +3.3 volt power supply (requires a separate via to power plane)
H5	VDD3.3	PWR	**Power I/O**: +3.3 volt power supply
H7	VSS	PWR	**Power VSS** (Thermal Ball)
H8	VSS	PWR	**Power VSS** (Thermal Ball)
H10	PIO3 PCS5#	I/O OUT	**Parallel I/O Bit [3] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [3] of the PIO register. This pin can also be used as peripheral chip select 5 (PCS5#) if PIO bit [3] is programmed for normal operation.
H11	PIO2 PCS6#	I/O OUT	**Parallel I/O Bit [2] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [2] of the PIO register. This pin can also be used as peripheral chip select 6 (PCS6#) if PIO bit [2] is programmed for normal operation.

Ball	Pin Name	Type	Description
H12	MCS[0]#	OUT	**Middle Memory Chip Select Output** (8ma Active LOW) These pins indicate to the system that a memory access is in progress to the midrange memory block. The base address and size of the mid-range memory block are programmable. The Middle memory chip selects are always configured for 16bit bus size. MCS[0]# can be programmed as the chip select for the entire middle chip select address range. MCS[0] is also used as CS_n for connecting a SDRAM externally.
H13	MCS[1]#	OUT	
H14	PIO24 MCS2#	I/O OUT	**Parallel I/O Bit [24] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [24] of the PIO register. This pin can also be used as middle chip select 2 (MCS2#) if PIO bit [24] is programmed for normal operation.
J1	CANRXD	IN	**CAN Receiver** (Schmitt Input with Pull-up) This pin connects to an external CAN transceiver receive pin.
J2	VSS	PWR	Power VSS
J3	CANTXD	OUT	**CAN Transmit** (2ma) This pin connects to an external CAN transceiver transmit pin.
J4	VSS	PWR	**Power VSS**
J5	TDI	IN	**Test Data Input** (Schmitt Trigger Input and Pull-up)
J10	PIO4 PCS4#	I/O OUT	**Parallel I/O bit 4 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [4] of the PIO register. This pin can also be used as peripheral chip select 4 (PCS4#) if PIO bit [4] is programmed for normal operation.
J11	PIO25 MCS3#	I/O OUT	**Parallel I/O Bit [25] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [25] of the PIO register. This pin can also be used as middle chip select 3 (MCS3#) if PIO bit [25] is programmed for normal operation.
J12	PIO16 LOCK# SRDYOUT	I/O OUT OUT	**Parallel I/O Bit [16] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit 16 of the PIO register. This pin can also be used as the CPU bus lock# output. If the SRDYOUT bit in the PLL/CLK register is set to '1', this pin outputs the internal SRDY signal for wait state debug use.
J13	RSTOUT#	OUT	**Reset Output** (4ma Active LOW) This pin indicates whether the CPU is being reset. It indicates that the internal logic is being reset and is to be used to reset any external peripherals.
J14	RSTIN#	IN	**Reset Input** (Schmitt Trigger Input, Active LOW with Pull-up) This pin causes the CPU to perform a reset. When this pin is asserted, the CPU immediately terminates any current bus cycles, resets internal logic and prepares for executing code at the reset address. FFFF0h in 20bit mode and FFFFE0h in 24bit mode. RSTIN# is synchronized internally and extended internally to allow ~200 ms for the DCR and RCR to settle to the values driven by there individual resistors. This input is provided with a Schmitt trigger to for power-on via an RC network.
K1	PIO31 I2CCLK	I/O I/O	**Parallel I/O Bit [31] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [31] of the PIO register. This pin can also be used with the I^2C block as the CLK if PIO bit 31 is programmed for normal operation.
K2	PIO13 I2CDTA	I/O	**Parallel I/O Bit [13] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [13] of the PIO register. This pin can also be used with the I^2C block as the I2CDTA if PIO bit [13] is programmed for normal operation.
K3	TEST#	IN	**TEST pin** (Schmitt Trigger Input and Pull-up) When this pin is pulled LOW, internal test modes may be input using address line 1 to 7. When HIGH, test is disabled.
K4	TD0	OUT	**Test Data Output** (4ma)
K5	VSS	PWR	**Power VSS**

Ball	Pin Name	Type	Description
K6	LCS#	IN	**Lower Chip Select** (Schmitt Trigger Input Active LOW with Pull-up) This pin is used by an external bus master to enable reading and writing the internal 256K bytes of SRAM.
K7	HLDA	OUT	**Hold Acknowledge** (4ma Active HIGH) This pin goes HIGH to indicate the bus has been released for use by an external bus master. The internal 256K bytes of internal memory is the only peripheral that can be accessed by an external bus master. The bus is requested using the HOLD pin (multiplexed on IO17).
K8	PIO30 INT5#	I/O IN	**Parallel I/O Bit [30] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [30] of the PIO register. This pin can also be used as INT5 when PIO30 is programmed for normal operation. **Note: This interrupt is shared with UART 3.**
K9	INT3	IN	**Interrupt In** (Schmitt Trigger Input, Active HIGH with Pull-down) These pins are external interrupt input requests. INT3 is OR'ed with the USB controller at interrupt type 15. INT1 is OR'ed with the MAC 1 controller at interrupt type 13.
K10	INT1	IN	
K11	VDD1.8	PWR	**Power Core**: +1.8 volt power supply
K12	PCS[3]#	OUT	**Peripheral Chip Select Output** (8ma Active LOW) These pins indicate to the system that a bus cycle is in progress to the corresponding region of the peripheral space. The base address of the peripheral block is programmable.
K13	PIO15 CAN1RXD	I/O IN	**Parallel I/O Bit [15] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [15] of the PIO register. This pin can also be used as CAN controller 1 receive if PIO bit [15] is programmed for normal operation.
K14	PIO14 CAN1TXD	I/O OUT	**Parallel I/O Bit [14] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [14] of the PIO register. This pin can also be used as CAN controller 1 transmit if PIO bit [14] is programmed for normal operation.
L1	TMS	IN	**Test Mode Select** (Schmitt Trigger Input and Pull-up)
L2	TCK	IN	**Test Clock** (Schmitt Trigger Input and Pull-up)
L3	TXEN	OUT	**Ethernet Transmit Enable** (4ma with Input and Pull-down)
L4	VDD1.8	PWR	**Power Core**: +1.8 volt power supply
L5	PIO17 HOLD	I/O IN	**Parallel I/O Bit [17] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [17] of the PIO register. This pin can also be used as the HOLD input if PIO bit [17] is programmed for normal operation. When driven HIGH by an external bus master, the CPU responds with HLDA and releases the bus for external use. Only the internal 256K bytes of memory are accessible externally.
L6	PIO0 TMR1IN	I/O IN	**Parallel I/O Bit [0] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [0] of the PIO register. This pin can also be used with Timer Channel 1 as TMR1IN if PIO bit [0] is programmed for normal operation.
L7	PIO11 TMR0IN	I/O IN	**Parallel I/O Bit 11 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [11] of the PIO register. This pin can also be used with Timer Channel 0 as TMR0IN if PIO bit [11] is programmed for normal operation.
L8	VSS	PWR	**Power VSS**
L9	PIO1 TMR1OUT	I/O OUT	**Parallel I/O Bit [1] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [1] of the PIO register. This pin can also be used with Timer Channel 1 as TMR1OUT if PIO bit [1] is programmed for normal operation.
L10	PIO10 TMR0OUT	I/O OUT	**Parallel I/O Bit [10] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [10] of the PIO register. This pin can also be used with Timer Channel 0 as TMR0OUT if PIO bit [10] is programmed for normal operation.

Ball	Pin Name	Type	Description
L11	PIO9 NMI	I/O IN	**Parallel I/O Bit [9] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [9] of the PIO register. This pin can also be used with NMI input if PIO bit [9] is programmed for normal operation.
L12	VSS	PWR	**Power VSS**
L13	PCS[2]#	OUT	**Peripheral Chip Select Output** (8ma Active LOW) These pins indicate to the system that a bus cycle is in progress to the corresponding region of the peripheral space. The base address of the peripheral block is programmable.
L14	PCS[0]#	OUT	**Peripheral Chip Select Output** (8ma Active LOW) These pins indicate to the system that a bus cycle is in progress to the corresponding region of the peripheral space. The base address of the peripheral block is programmable.
M1	TRST#	IN	**Test Reset** (Schmitt Trigger Input and Pull-up)
M2	TCLK	IN	**Ethernet Transmit Clock** (4ma with Input and Pull-down)
M3	TXER	OUT	**Ethernet Transmit Error** (4ma with Input and Pull-down)
M4	RXCLK	IN	**Ethernet Receive Clock** (4ma with Input and Pull-down)
M5	RXER	IN	**Ethernet Receive Error** (4ma with Input and Pull-down)
M6	RXDV	IN	**Ethernet Receive Data Valid** (4ma with input and Pull-down)
M7	PIO6 ARDY	I/O IN	**Parallel I/O Bit 6 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [6] of the PIO register. This pin can also be used with an external ready source ARDY if PIO bit [6] is programmed for normal operation. ARDY is double synchronized internally using the falling edge of CPUCLK. It can be used to extend external accesses if enabled by the appropriate registers (External Ready).
M8	VDD3.3	PWR	**Power I/O**: +3.3 volt power supply
M9	PIO8 DRQ3	I/O IN	**Parallel I/O Bit [8] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [8] of the PIO register. This pin can also be used with DMA channel 3 as DRQ3 if PIO bit [8] is programmed for normal operation.
M10	PIO7 DRQ2	I/O IN	**Parallel I/O Bit [7] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [7] of the PIO register. This pin can also be used with DMA channel 2 as DRQ2 if PIO bit [7] is programmed for normal operation.
M11	PIO29 DRQ1	I/O IN	**Parallel I/O Bit [29] and DRQ1 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [29] of the PIO register. This pin can also be used as DMA request 1 with the DMA if PIO bit [29] is programmed for normal operation.
M12	PIO12 DRQ0	I/O IN	**Parallel I/O Bit 12 Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [12] of the PIO register. This pin can also be used with DMA channel 0 as DRQ0 if PIO bit [12] is programmed for normal operation.
M13	VDD3.3	PWR	**Power I/O**: +3.3 volt power supply
M14	VSS	PWR	**Power VSS**
N1	MDC	OUT	**Ethernet MII 1 Clock Out** (4ma with Input and Pull-down)
N2	TXD[3]	OUT	**Ethernet Transmit Data Bus Bit [3]** (4ma with input and Pull-down)
N3	TXD[1]	OUT	**Ethernet Transmit Data Bus Bit [1]** (4ma with Input and Pull-down)
N4	RXD[3]	IN	**Ethernet Receive Data Bus Bit [3]** (4ma with Input and Pull-down)
N5	RXD[1]	IN	**Ethernet Receive Data Bus Bit [1]** (4ma with input and Pull-down)
N6	RXCOl	IN	**Ethernet Receive Collision** (4ma with Input and Pull-down)
N7	PIO28 RXD3 SDI	I/O IN IN	**Parallel I/O Bit [28] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [28] of the PIO register. This pin can also be used with: ● UART 3 as receive data (RXD3) if PIO bit [28] is programmed for normal operation. ● The SPI controller if the SPIEN bit is set in the DCR register. This pin connects to the serial data in (SDI) of the SPI controller.

Ball	Pin Name	Type	Description
N8	PIO18 CTS3# SLVSEL#	I/O IN IN	**Parallel I/O Bit [18] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit 18 of the PIO register. This pin can also be used with: ● UART 3 as clear to send (CTS3#) if PIO bit [18] is programmed for normal operation. ● The SPI controller if the SPIEN bit is set in the DCR register. This pin connects to the slave select input (SLVSEL#) of the SPI controller.
N9	PIO23 RXD2	I/O IN	**Parallel I/O Bit [23] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [23] of the PIO register. This pin can also be used with UART 2 as receive data (RXD2) if PIO bit [23] is programmed for normal operation.
N10	PIO21 CTS2#	I/O IN	**Parallel I/O Bit [21] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [21] of the PIO register. This pin can also be used with UART 2 as Clear to Send (CTS2#) if PIO bit [21] is programmed for normal operation.
N11	RXD1	IN	**Receive Data 1 In** (Schmitt Trigger Input, Active HIGH with Pull-up) This pin provides serial receive data from the system to serial port 1.
N12	CTS1#	IN	**Clear to Send 1 In** (Schmitt Trigger Input, Active HIGH with Pull-up) This pin provides the Clear to Send input for serial port 1. This pin provides the handshaking input for serial port 1.
N13	RXD0	IN	**Receive Data 0 In** (Schmitt Trigger Input, Active HIGH with Pull-up) This pin provides serial receive data from the system to serial port 0.
N14	CTS0#	IN	**Clear to Send 0 In** (Schmitt Trigger Input, Active High with Pull up) This pin provides the Clear to Send input for serial port 0. This pin provides the handshaking input for serial port 0.
P1	MDIO	I/O	**Ethernet MII 1 Management Data** (4ma with Input and Pull-down)
P2	TXD[2]	OUT	**Ethernet Transmit Data Bus Bit [2]** (4ma with input and Pull-down)
P3	TXD[0]	OUT	**Ethernet Transmit Data Bus Bit [0]** (4ma with Input and Pull-down)
P4	RXD[2]	IN	**Ethernet Receive Data Bus Bit [2]** (4ma with input and Pull-down)
P5	RXD[0]	IN	**Ethernet Receive Data Bus Bit [0]** (4ma with input and Pull-down)
P6	RXCRS	IN	**Ethernet Receive Carrier Sense** (4ma with Input and Pull-down)
P7	PIO27 TXD3 SDO	I/O OUT OUT	**Parallel I/O Bit [27] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [27] of the PIO register. This pin can also be used with: ● UART 3 as transmit data (TXD3) if PIO bit [27] is programmed for normal operation. ● The SPI controller if the SPIEN bit is set in the DCR register. This pin connects to the serial data out (SDO) of the SPI controller.
P8	PIO19 RTS3# SCK	I/O OUT I/O	**Parallel I/O Bit [19] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [19] of the PIO register. This pin can also be used with: ● UART 3 as ready to send (RTS3#) if PIO bit [19] is programmed for normal operation. ● The SPI controller if the SPIEN bit is set in the DCR register. This pin connects to the serial clock (SCK) of the SPI controller.
P9	PIO22 TXD2	I/O OUT	**Parallel I/O Bit [22] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [22] of the PIO register. This pin can also be used with UART 2 as transmit data (TXD2) if PIO bit [22] is programmed for normal operation.
P10	PIO20 RTS2#	I/O OUT	**Parallel I/O Bit [20] Pin** (4ma Schmitt Input with Pull-up) This pin corresponds to bit [20] of the PIO register. This pin can also be used with UART 2 as ready to send (RTS2#) if PIO bit [20] is programmed for normal operation.
P11	TXD1	OUT	**Transmit Data 1 Out** (2ma) This pin provides serial transmit data to the system from serial port 1.
P12	RTS1#	OUT	**Ready to Send 1 Out** (2ma) This pin provides the Ready to Send output for serial port 1. This pin provides the handshaking output for serial port 1.

Ball	Pin Name	Type	Description
P13	TXD0	OUT	**Transmit Data 0 Out** (2ma) This pin provides serial transmit data to the system from serial port 0.
P14	RTS0#	OUT	**Ready to Send 0 Out** (2ma) This pin provides the Ready to Send output for serial port 0. This pin provides the handshaking output for serial port 0.